150 mA, Low I_Q, Low-Dropout Regulator for Portables

Check for Samples: TLV717

FEATURES

- **Very Low Dropout: 250 mV at 150 mA**
- **Accuracy: 0.5% (typical)**
- **Low I_Q: 35 μA**
- **Available in Fixed-Output Voltages: 1.2 V to 5.0 V**
- **High PSRR:**
  - **70 dB at 1 kHz**
  - **50 dB at 1 MHz**
- **Stable with Effective Output Capacitance: 0.1 μF**
- **Foldback Current Limit**
- **Package: 1-mm × 1-mm DFN**

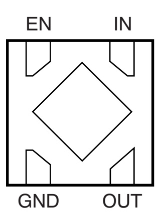
(1) See the Package Option Addendum at the end of this document for a complete list of available voltage options.

(2) See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.

APPLICATIONS

- **Wireless Handsets, Smart Phones, PDAs**
- **MP3 Players**
- **Other Hand-Held Products**

TLV717x
1-mm x 1-mm DQN
(Bottom View)



DESCRIPTION

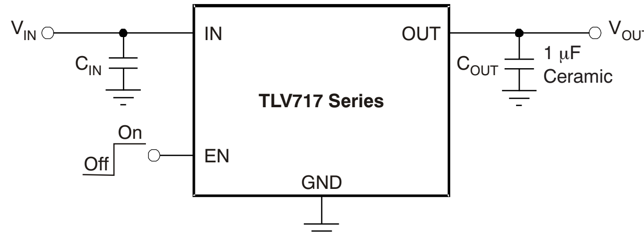
The TLV717xx series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 0.5%.

The TLV717xx series offer current foldback which throttles down the output current with a decrease in load resistance. The typical value at which current foldback kicks in is 350 mA; the typical value of the output short current limit value is 40 mA.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 μF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV717xx series is available in a 1-mm × 1-mm DQN package that makes them ideal for hand-held applications. The TLV717xxP provides an active pull-down circuit to quickly discarge output loads.

Typical Application Circuit



PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TLV717**xx(x) P yyy z**	**XX(X)** is nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 475 = 4.75 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is package designator. **Z** is package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –25°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	Input range, V_{IN}	–0.3	6.0	V
	Enable range, V_{EN}	–0.3	V_{IN} + 0.3	V
	Output range, V_{OUT}	–0.3	6.0	V
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation, P_{DISS}		See Thermal Information table		
Temperature	Junction range, T_J	–55	+150	°C
	Storage junction range, T_{stg}	–55	+150	°C
Electrostatic discharge rating	Human body model (HBM)		2000	V
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV71713PDQN DQN 4 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	393.3	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	140.3	
θ_{JB}	Junction-to-board thermal resistance	330	
ψ_{JT}	Junction-to-top characterization parameter	6.5	
ψ_{JB}	Junction-to-board characterization parameter	329	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 μF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TLV717 MIN	TLV717 TYP	TLV717 MAX	UNIT
V_{IN}	Input voltage range			1.7		5.5	V
V_{OUT}	Output voltage range			1.2		5.0	V
I_{OUT}	Output current			150			mA
	DC output accuracy	T_A = +25°C			0.5		%
	DC output accuracy	V_{OUT} ≥ 1.2 V, –40°C ≤ T_A ≤ +85°C		–1.5		+1.5	%
	DC output accuracy	V_{OUT} ≤ 1.2 V				25	mV
$\Delta V_O/V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V			1	5	mV
$\Delta V_O/I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	20	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 150 mA	1.2 V ≤ V_{OUT} < 1.8 V		330	450	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 150 mA	1.8 V ≤ V_{OUT} ≤ 5.0 V		215	350	mV
I_{GND}	Ground pin current	I_{OUT} = 0 mA			35	55	μA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V			0.1	0.5	μA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA	f = 10 Hz		75		dB
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA	f = 100 Hz		75		dB
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA	f = 1 kHz		75		dB
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA	f = 10 kHz		60		dB
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA	f = 100 kHz		50		dB
V_{NOISE}	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			55		μV_{RMS}
t_{STR}	Startup time	C_{OUT} = 1.0 μF, I_{OUT} = 150 mA			100		μs
I_{SC}	Short current limit	V_{IN} = min ($V_{OUT(NOM)}$ + 1 V, 5.5 V), V_{OUT} = 0 V			40		mA
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		μA
$R_{PULLDOWN}$	Pull-down resistor (TLV717P only)				120		Ω
UVLO	Undervoltage lockout	V_{IN} rising			1.6		V
T_J	Operating junction temperature range			–40		+125	°C

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DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS

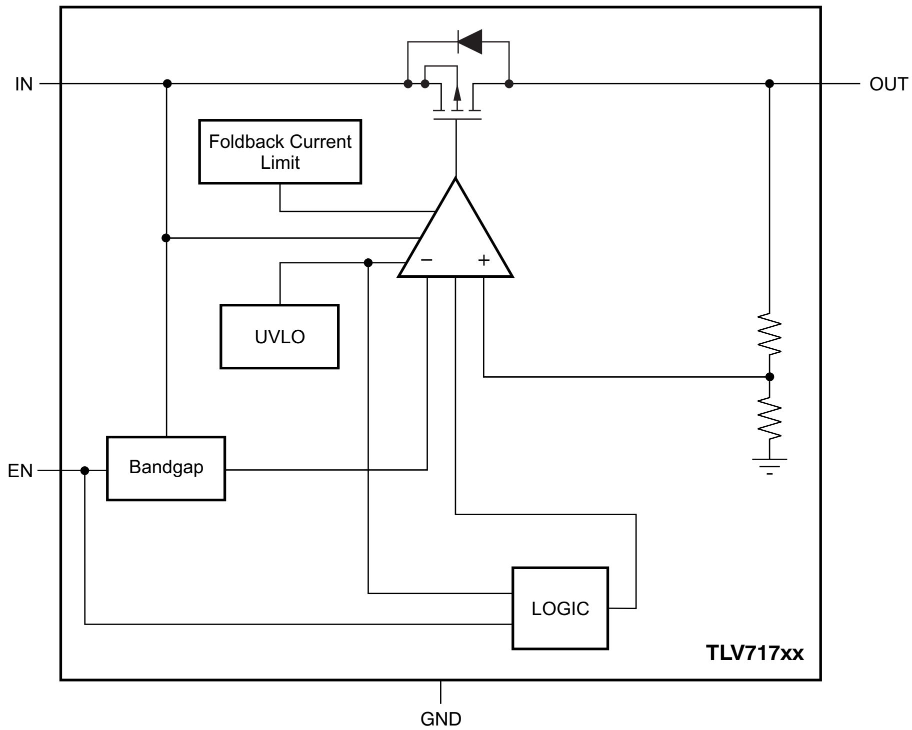


Figure 1. TLV717xx Block Diagram

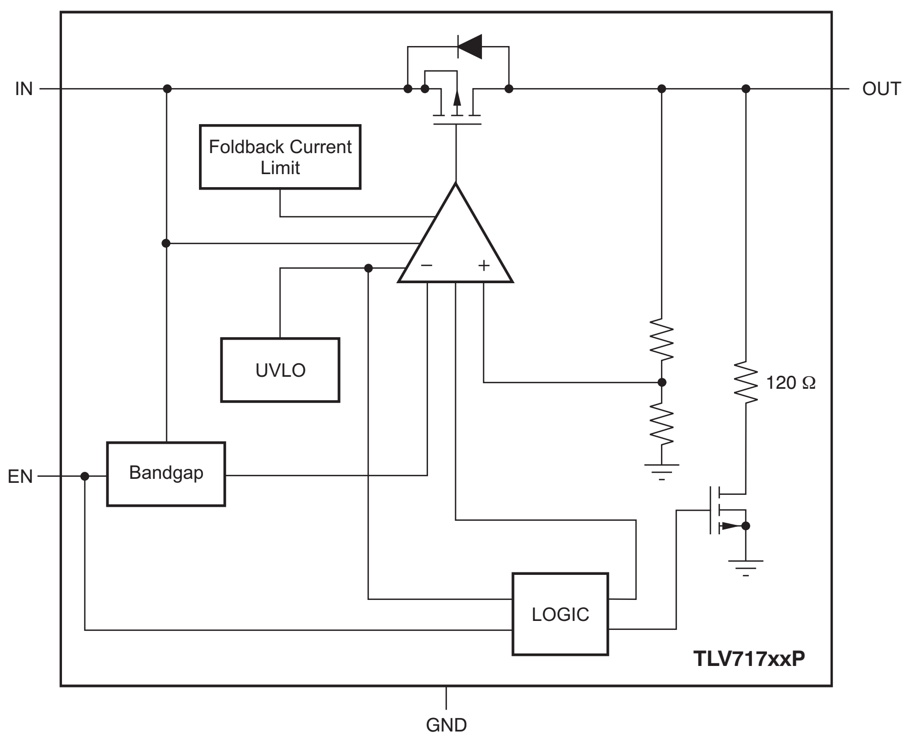
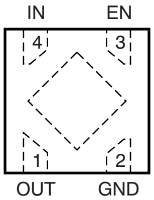


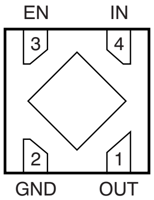
Figure 2. TLV717xxP Block Diagram

PIN CONFIGURATIONS

DQN PACKAGE
1-mm × 1-mm TBD
(Top View)



DQN PACKAGE
1-mm × 1-mm TBD
(Bottom View)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NO.	NAME	
1	OUT	Regulated output voltage pin. A small 1-μF ceramic capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
2	GND	Ground pin
3	EN	Enable pin. Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
4	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
—	Thermal pad	This pin can be left open or tied to any voltage between GND and IN. It is recommended to connect this pin to GND to minimize noise and maximize thermal performance.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, $V_{IN} = V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, $V_{EN} = V_{IN}$, and C_{OUT} = 1 μF, unless otherwise noted.

LOAD REGULATION

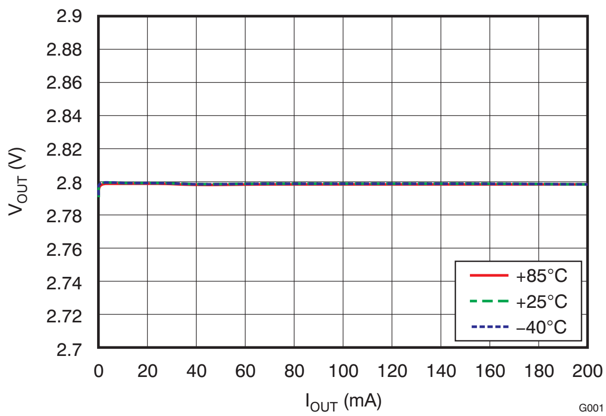


Figure 3.

LINE REGULATION

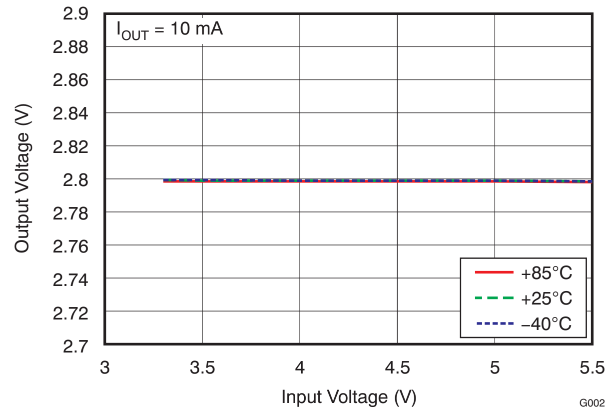


Figure 4.

LINE REGULATION

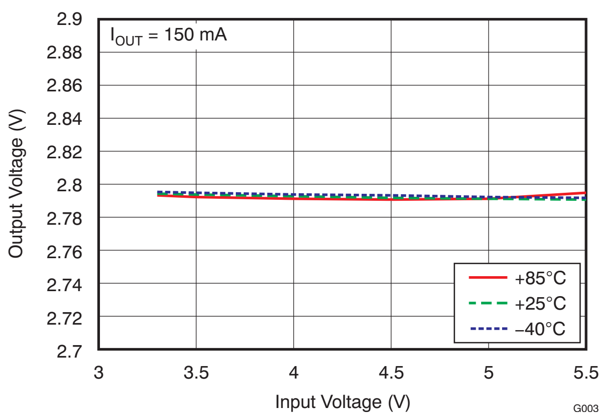


Figure 5.

DROPOUT VOLTAGE vs INPUT VOLTAGE

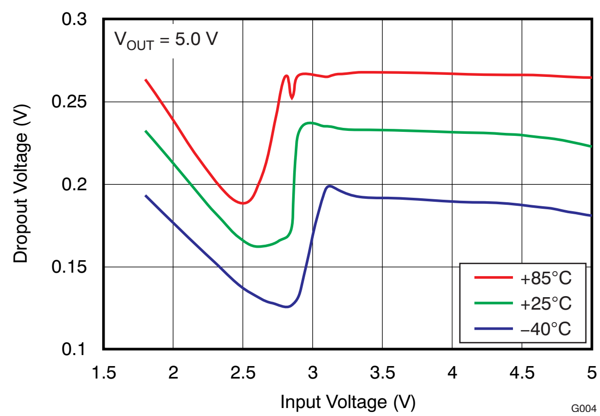


Figure 6.

DROPOUT VOLTAGE vs OUTPUT CURRENT

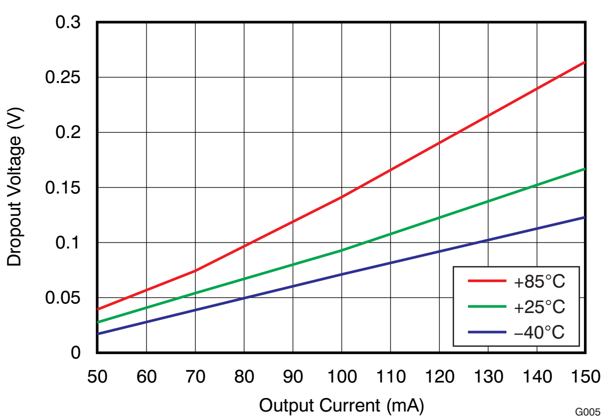


Figure 7.

OUTPUT VOLTAGE vs TEMPERATURE

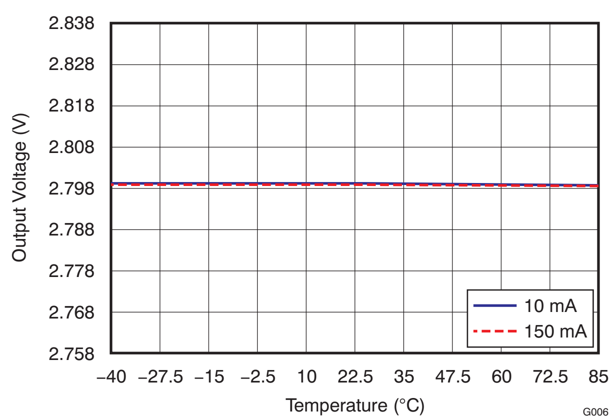


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 μF, unless otherwise noted.

GROUND PIN CURRENT vs INPUT VOLTAGE

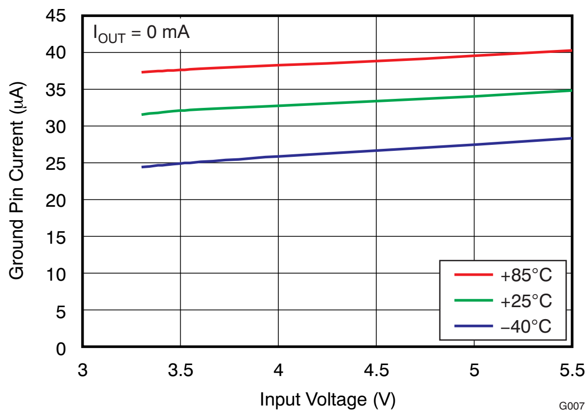


Figure 9.

GROUND PIN CURRENT vs OUTPUT CURRENT

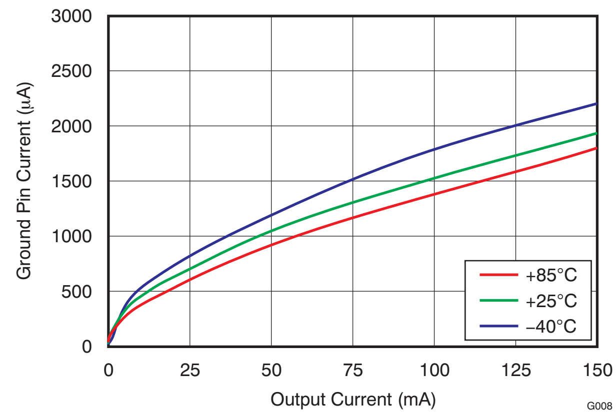


Figure 10.

GROUND PIN CURRENT vs TEMPERATURE

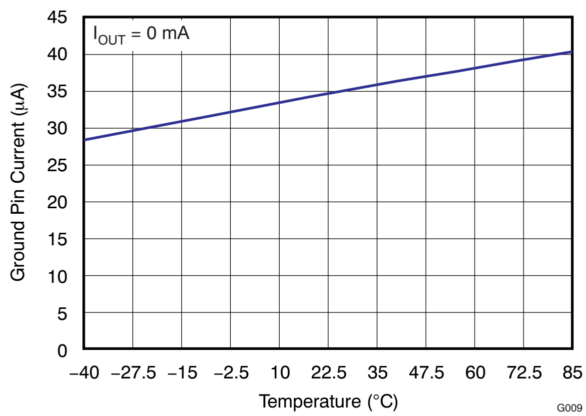


Figure 11.

OUTPUT VOLTAGE vs OUTPUT CURRENT

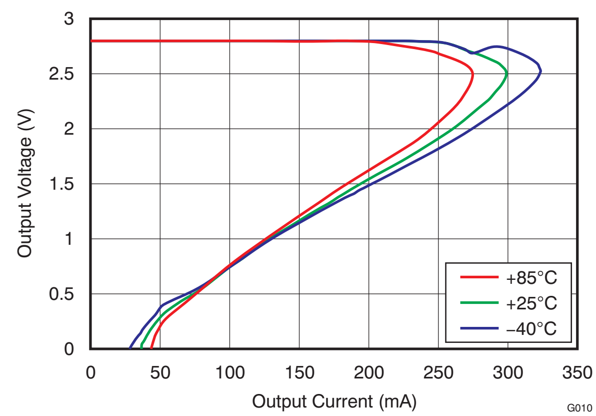


Figure 12.

TLV71728
PSRR vs FREQUENCY

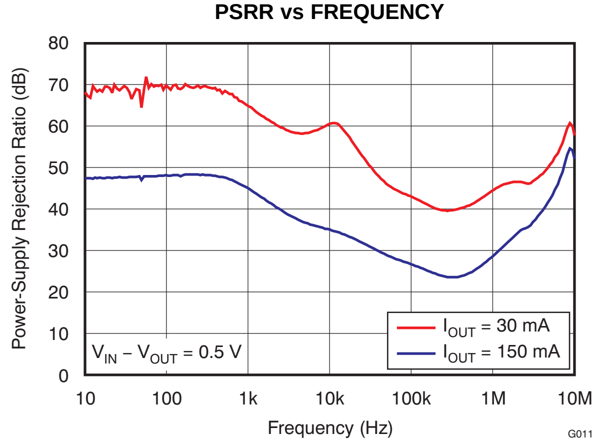


Figure 13.

TLV71728
PSRR vs FREQUENCY

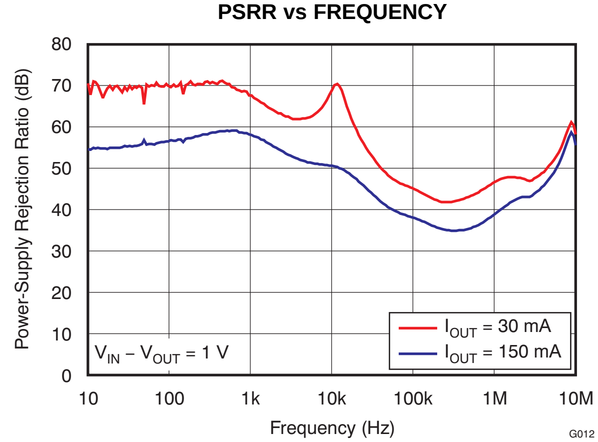


Figure 14.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 μF, unless otherwise noted.

PSRR vs INPUT VOLTAGE

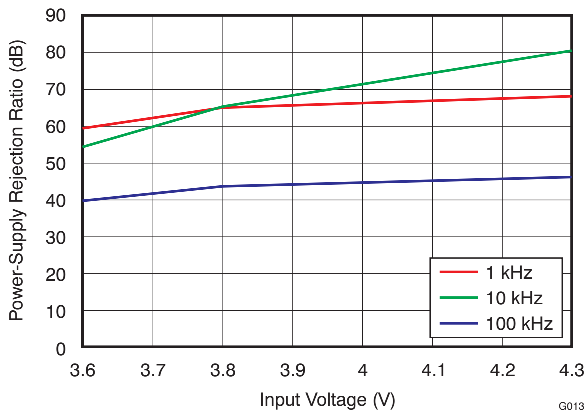


Figure 15.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

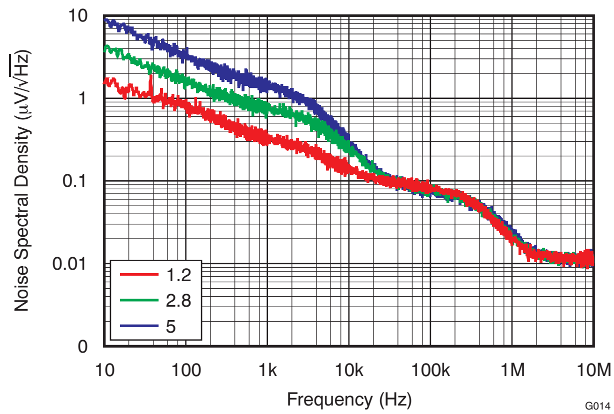


Figure 16.

PRODUCT PREVIEW

APPLICATION INFORMATION

The TLV717xx belongs to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current foldback. Operating junction temperature of the device is –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. The TLV717xx is designed to be stable with an effective capacitance of 0.1 µF or larger at the output, though a 1-µF ceramic capacitor is recommended for typical applications. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications. Note that using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

INTERNAL CURRENT LIMIT

The TLV717xx has an internal foldback current limit that helps to protect the regulator during fault conditions. The current supplied by the device is gradually throttled down as the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The advantage of foldback current limit is that the I_{LIMIT} value is less than the fixed current limit. Therefore, the power that the PMOS pass transistor dissipates (V_{IN} – V_{OUT}) × I_{LIMIT} is much less.

The PMOS pass element in the TLV717xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 0.9 V. This relatively lower value of voltage that is required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

PRODUCT PREVIEW

DROPOUT VOLTAGE

The TLV717xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude but increases the duration of the transient response.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV717xx uses an undervoltage lockout circuit (UVLO = 1.6 V) to keep the output shut off until internal circuitry is operating properly.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC low and high-K boards are given in the Thermal Information table. Using heavier copper increases the effectiveness in removing heat from the device. The addition, plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLV71712PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71712PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71713PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71713PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71715PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71715PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71718PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71718PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71725PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71725PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV717285PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV717285PQNR	PREVIEW	X2SON	DQN	5	3000	TBD	Call TI	Call TI	
TLV71728PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71728PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71730PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71730PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71733PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/ Ball Finish	MSL Peak Temp [(3)]	Samples (Requires Login)
TLV71733PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71736PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV71736PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

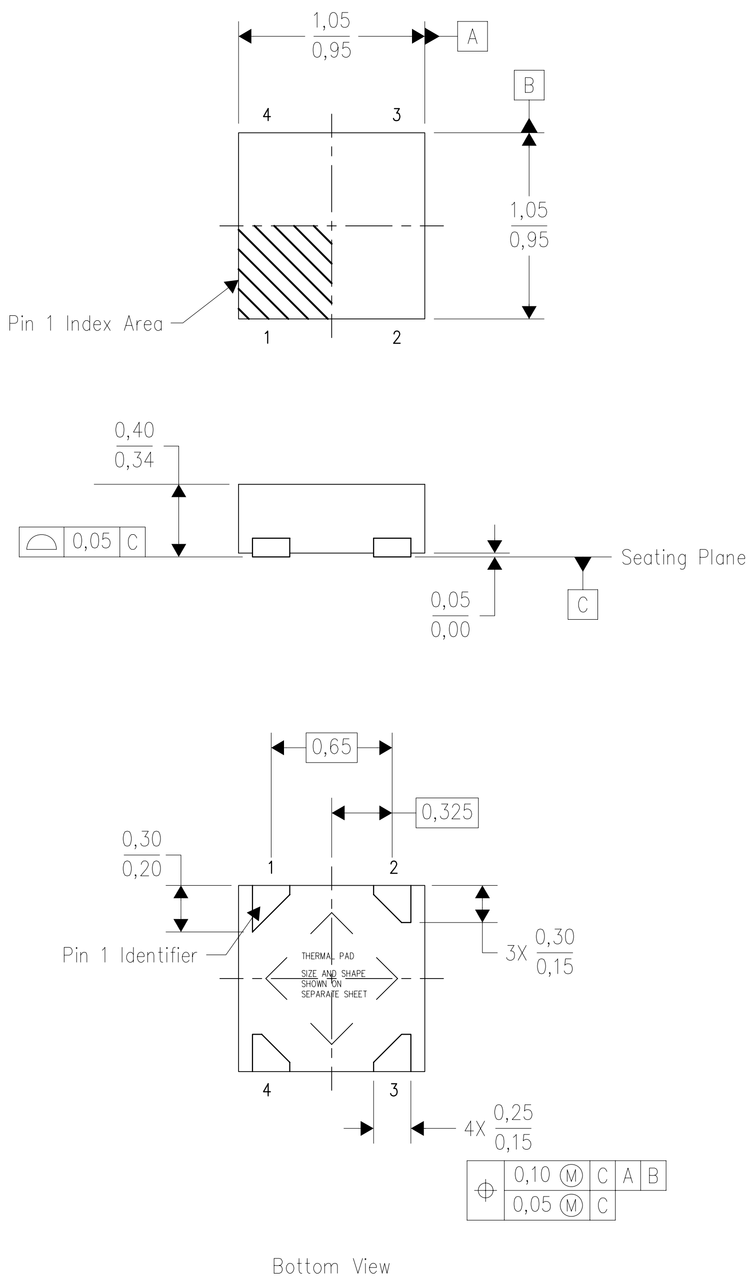
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DQN (S-PX2SON-N4) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.